DIGITAL LOGIC DESIGN LAB

REPORT

ECE 1003 L 21-22

WIN 2022-2023.

Name: SWARNLATA

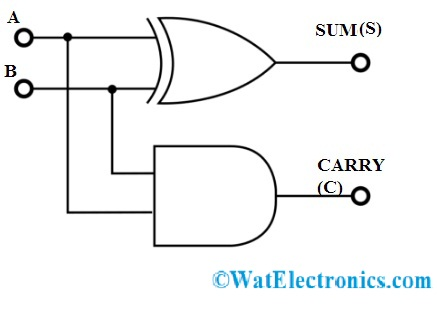
EXPERIMENT -2

**HALF ADDER**

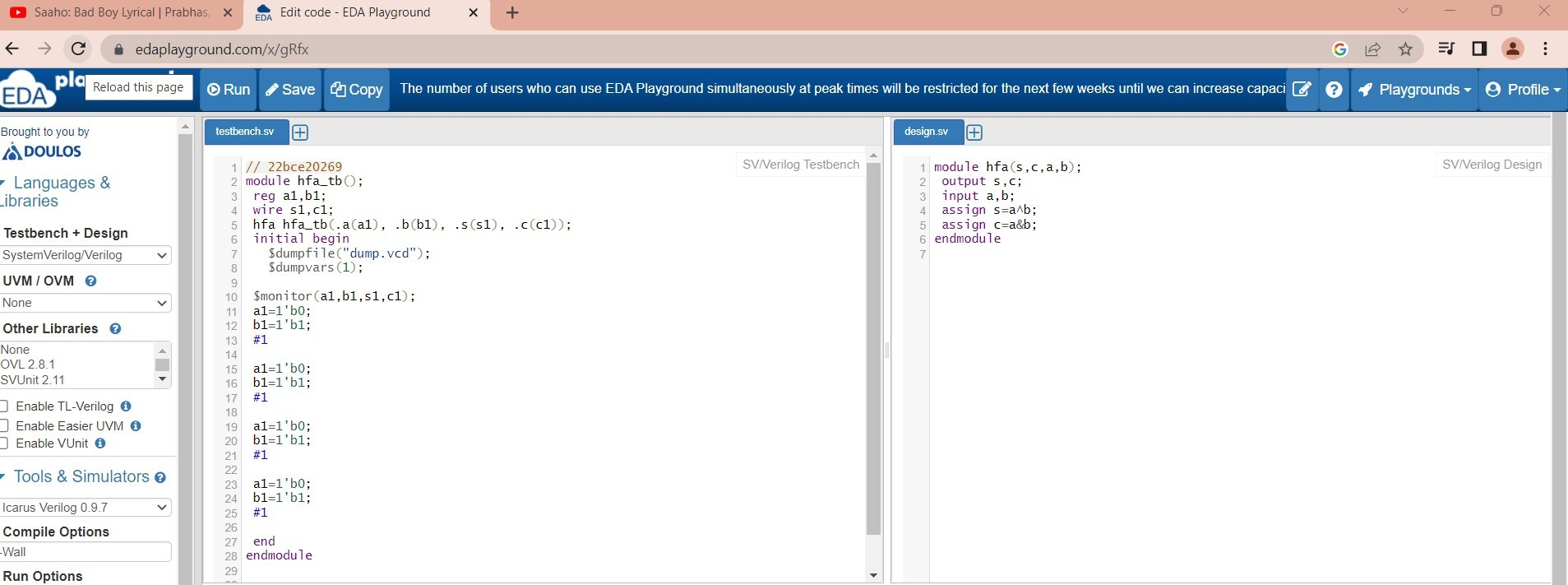
**OBJECTIVE:**Verification of half adder

**THEORY:**half adder is a combinational logic circuit

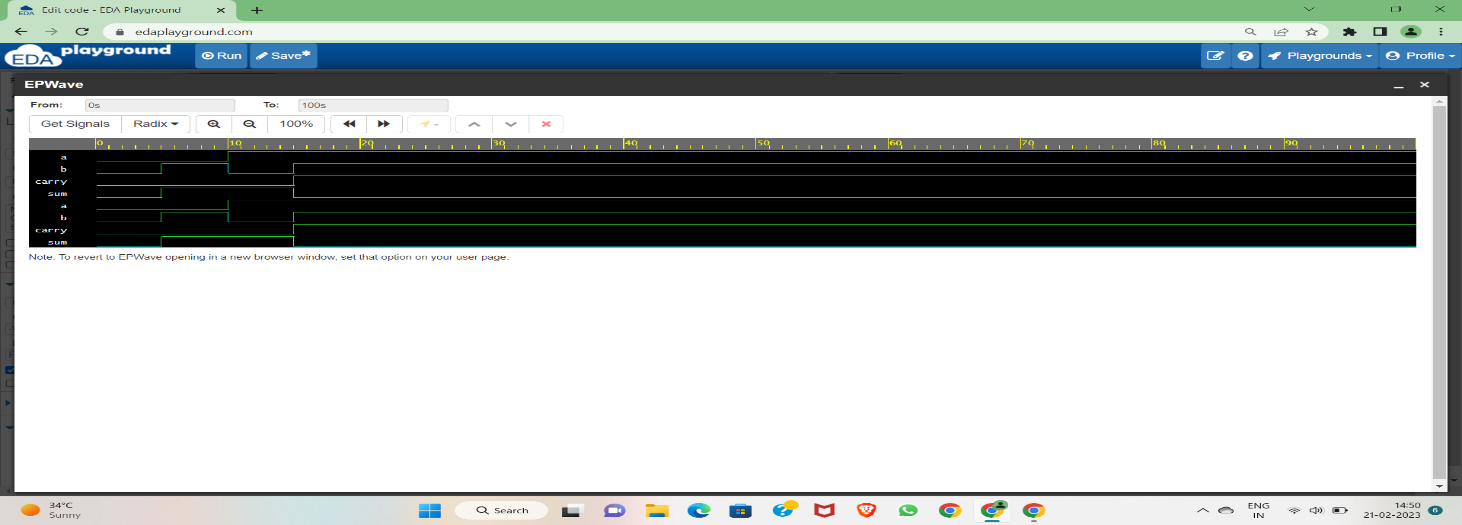
**BLOCK DIAGRAM:**



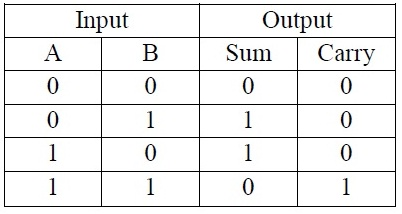
**IMPLEMENTATION AND OUTPUT:**



**WAVE FORM:**



**OBSERVATION:**

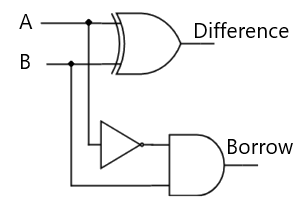


**HALF SUBTRACTOR**

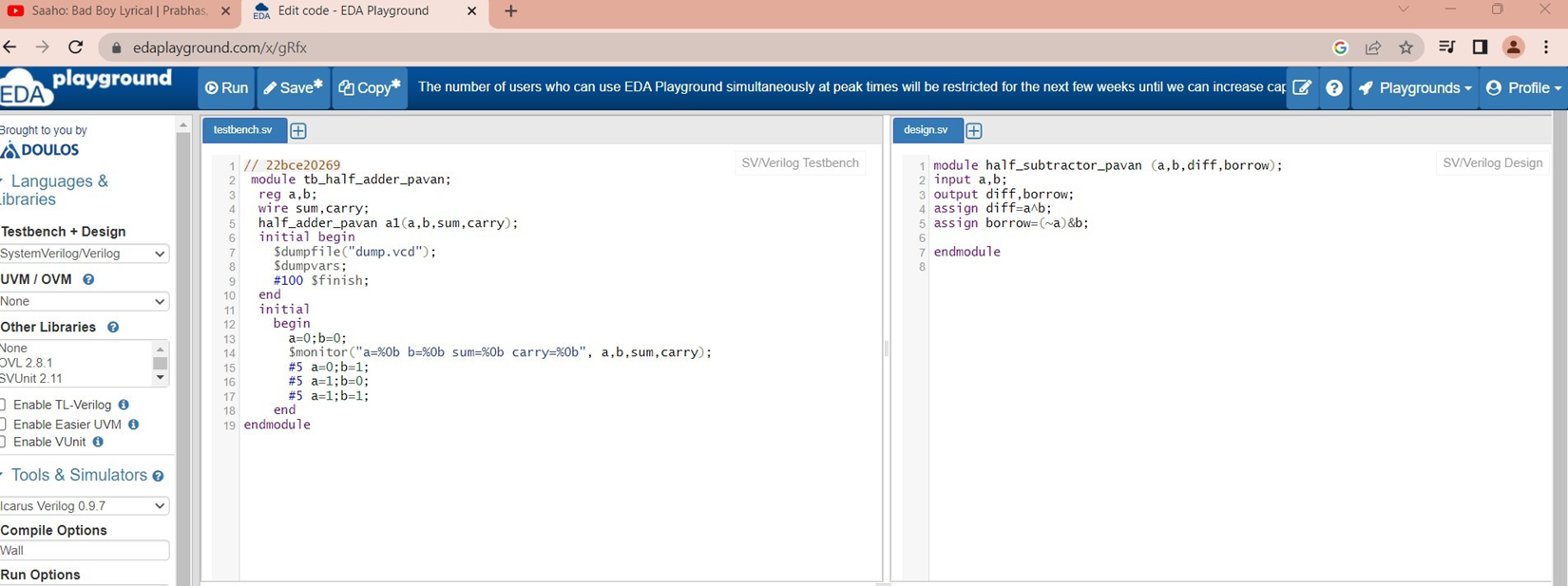
**OBJECTIVE:**Verification of half subtractor

**THEORY:**Half subtractor is a combinational logic gate

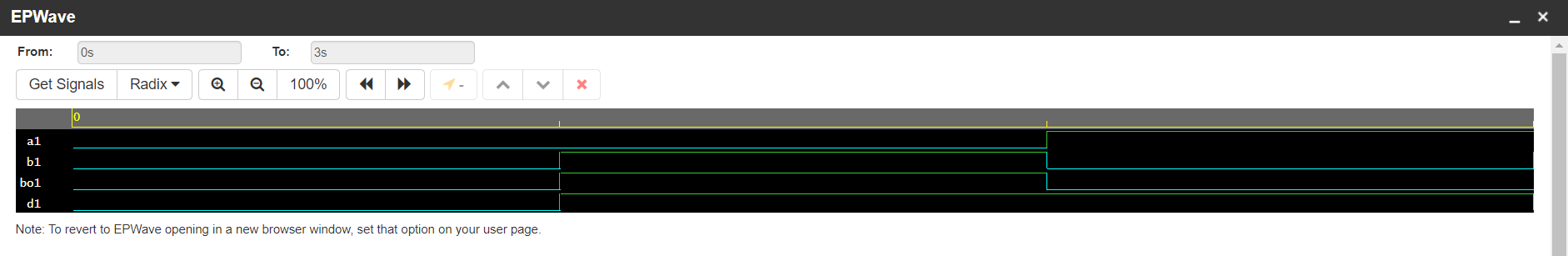
**BLOCK DIAGRAM:**



**IMPLEMENTATION AND OUTPUT:**

****

**WAVE FORM:**



**OBSERVATION:**

